

Abstract of the Invention

A format conversion circuit 100 includes a FIFO memory 101 for writing and reading video data VD in synchronization with a sampling clock CK, a header generation circuit 102 for generating an MPEG2-TS packet header, and a synchronous timing detection circuit 103 for detecting a horizontal synchronizing signal for the video data VD. The format conversion circuit 100 also includes a counter 104 which counts the number of bytes of packet header and the number of bytes of video data VD, and a switch 105 which selects the packet header until the counted number of bytes reaches four bytes, and then selects the video data read out of the FIFO memory 101.

[Selected Drawing] Fig. 8